CLAIMS

What is claimed is:

1. A system comprising:

a system memory controller; and

a first memory module comprising:

a first memory module controller coupled to the system memory controller; and

a first plurality of memory devices coupled to the first memory module controller.

2. The system of claim 1, further comprising a first memory bus coupled between the system first memory module and the first memory module controller.

3. The system of claim 2, wherein the first memory bus comprises a clock signal.

4. The system of claim 2, wherein the first memory bus comprises a handshake signal that indicates when the first memory module controller is communicating data to the system memory controller.

5. The system of claim 2, further comprising a second memory bus coupled between first memory module controller and the first plurality of memory devices.

6. The system of claim 5, wherein the second memory bus comprises a clock signal.

7. The system of claim 5, wherein the first memory bus operates at a first data rate and the second memory bus operates at a second data rate, wherein the first data rate is different than the second data rate.

8. The system of claim 5, wherein the first memory bus has a first number of signal lines and the second memory bus has a second number of signal lines, wherein the first number of signal lines is different than the second number of signal lines.

9. The system of claim 5, wherein the first memory module controller comprises:

request handling circuitry structured to receive a first memory transaction from the first memory bus; and

control logic coupled to the request handling circuitry and generating a second memory transaction on the second memory bus corresponding to the first memory transaction on the first bus.

10. The system of claim 2, wherein the first memory bus carries time-multiplexed data and address information, and the second memory bus includes separate address and data lines.

11. The system of claim 1, wherein the first memory module is a dual in-line first memory module (DIMM).

12. The system of claim 1, wherein the first memory module is a single in-line first memory module (SIMM).

13. The system of claim 1, wherein the first plurality of memory devices comprise volatile memory devices.

14. The system of claim 1, wherein the first plurality of memory devices comprise nonvolatile memory devices.

15. The system of claim 1, further comprising a second memory module comprising:

a second memory module controller coupled to the system memory controller; and

a second plurality of memory devices coupled to the second memory module controller.

16. The system of claim 15, wherein the first plurality of memory devices stores data in a different way than the second plurality of memory devices.

17. A system comprising:

a system memory controller;

a memory bus coupled to the system memory controller; and

a memory comprising:

a memory module controller coupled to the memory bus; and

a plurality of memory devices coupled to the memory module controller, wherein the memory module controller receives a first memory transaction from the memory bus in a first format and provides a second memory transaction in a second format to at least one of the second plurality of memory devices.

18. A method of communicating a memory transaction between a system memory controller and at least one of a plurality of memory devices on a memory module including a memory module controller, the method comprising the steps of:

sending a memory transaction from the system memory controller to the memory module controller, the memory transaction having a first format;

reformatting the memory transaction for the at least one of the memory devices; and

sending the reformatted memory transaction to the at least one of the memory devices.

19. The method of claim 18, wherein the memory transaction is a read transaction.

20. The method of claim 18, wherein the memory transaction is a write transaction.

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